In the Specification:

Amend the paragraph found on page 11 as follows:

According to a further aspect of the invention, low speed signals are transmitted through the connectors 46 and 44 in a manner such that the inversion of the modules relative to each other is transparent. Referring to Figure 7, low speed signals are designated "Signal A", "Signal B", etc., to "Signal Z". When inverted, Signal Z is transmitted on the pin carrying Signal A when uninverted, and Signal Y is transmitted on the pin carrying Signal B when uninverted, etc. A signal "INVERTED_N" occupies the top left corner of the connector 46 pinout diagram in Figure 7. The corresponding connector pin 44 on the motherboard is coupled to a pull-up resistor 51 (Fig. ~~9~~ 10). When the connector 46 is plugged into the connector 44 in the non-inverted position (e.g. for the XFP module 34), the INVERTED_N signal on the motherboard 32 is high. When the connector 46 is plugged into the connector 44 in the inverted position, the ground connection GND in the lower right of Figure 7 pulls the INVERTED_N signal low. So, the INVERTED_N signal can be used by logic on the motherboard 32 to decode which low speed signals are present on which pins on the connector 44. For example, referring to Figure 9, there may be for example a PLD 100 on the motherboard 32. The low speed signals such as Signal A, Signal B, etc. may be general purpose I/O signals. The PLD 100 receives the low speed signals and the INVERTED_N signal. If the INVERTED_N signal is high, the PLD recognizes the low speed signals as shown in Figure 9A – Signal A through Signal Z. If the INVERTED_N signal is low, the PLD 100 recognizes the low speed signals as shown in Figure 9B – Signal Z through Signal A.